IN THE CLAIMS

Please amend the claims as indicated below.

1. (currently amended) A driver circuit, comprising:

a driver configured to switch a current source and a current sink to a load via a single node; and

a predriver having first and second cross-coupled inverters responsive to an input signal, the first inverter being configured to control the switching of the current source to the load and the second inverter being configured to control the switching of the current sink to the load, wherein the cross-coupling between the first and second inverters and buffer connections of the first and second inverters to said driver are ~~is~~ configured such that the first inverter controls the driver to remove~~s~~ the current source from the load via said single node before the second inverter controls the driver to switch~~es~~ the current sink to the load via said single node in response to a transition in the input signal such that a crow-bar current is controlled, and conversely the second inverter controls the driver to remove~~s~~ the current sink from the load via said single node before the first inverter controls the driver to switch~~es~~ the current source to the load via said single node in response to an opposite transition in the input signal such that said crow-bar current is controlled, and wherein the first and second inverters are further configured to remove both the current source and the current sink from the load concurrently to allow tristate operation of the driver.

2. (original) The driver circuit of claim 1 wherein each of the inverters comprises a pair of transistors connected in series.

3. (original) The driver circuit of claim 2 wherein each of the transistors comprises a field effect transistor (FET).

4. (original) The driver circuit of claim 1 wherein each of the inverters comprises a p-channel FET (PFET) having a drain and a n-channel FET (NFET) having a drain connected to the drain of the PFET.

5. (original) The driver circuit of claim 4 wherein for each of the inverters, the NFET comprises a gate responsive to the input signal, and the PFET comprises a gate coupled to the drain of the PFET in the other inverter.

6. (original) The driver circuit of claim 5 wherein for each of the inverters, the NFET is larger than the PFET.

7. (original) The driver circuit of claim 5 wherein the NFET in the first inverter is substantially the same size as the NFET in the second inverter, and wherein the PFET in the first inverter is substantially the same size as the PFET in the second inverter.

8. (previously presented) The driver circuit of claim 1 further comprising a voltage source coupled to the inverters, the voltage source providing level shifting at an output of each inverter in response to the input signal.

9. (canceled)

10. (currently amended) A driver circuit, comprising:

an input inverter configured to receive an input signal;

two cross-coupled inverters that include a first and second NFET and a first and second PFET, wherein the first NFET is configured to receive the output of the input inverter, and wherein the second NFET is configured to receive the input signal;

first and second output buffers configured to receive first and second outputs of the two cross-coupled inverters, wherein said first buffer

inverts said first output and said second buffer leaves said second output uninverted;

wherein the NFETs of the cross-coupled inverters are larger than the PFETs of the cross-coupled inverters, said NFETs and PFETs being sized with respect to each other such that a first break before make delay is created between a first predriver output signal at a first predriver output node and a second predriver output signal at a second predriver output node; and a second break before make delay is created between the second predriver output signal at the second predriver output node and the first predriver output signal at the first predriver output node; and

first and second tristate devices configured to disable output signals of the first and second predriver output nodes.

11. (original) The driver circuit of Claim 10, wherein each of the input inverter, the cross-coupled inverters and the first and second output buffers are sized with respect to each other such that first and second delays between the input signal and predriver make signals on a rising and falling edge, respectively, are substantially equal; and

wherein each of the input inverter, the cross-coupled inverters and the first and second output buffers are further sized with respect to each other such that third and fourth delays between a break signal and make signal on a rising edge and on a falling edge, respectively, are substantially equal.

12. (original) The driver circuit of Claim 10, wherein the PFETs of the cross-coupled inverters are substantially equal in size.

13. (canceled)

14. (previously presented) The driver circuit of Claim 10, wherein each tristate device is a logic gate, and wherein each logic gate includes a first input

configured to receive a predriver output signal, each logic gate being further configured to receive a disable signal.

15. (original) The driver circuit of Claim 14, wherein the first tristate device is a NAND gate and the second tristate device is a NOR gate.

16. (previously presented) The driver circuit of Claim 10, wherein the first tristate device is an NFET and the second tristate device is a PFET.

17. (original) The driver circuit of Claim 10, further comprising:

an output driver device configured to receive the first and second predriver output signals, the output driver device being further configured to drive a capacitive load.

18. (original) The driver circuit of Claim 17, wherein each of the input inverter, the cross-coupled inverters and the first and second output buffers are further sized so as to be sufficiently large to drive the capacitive load.

19. (original) The driver circuit of Claim 17, wherein the output driver device includes an NFET device and a PFET device.

20. (original) The driver circuit of Claim 10, wherein the input signal has an input voltage, and the predriver further comprises:

a voltage supply configured to supply, at said predriver output nodes, a higher voltage than said input voltage.

21. (original) The driver circuit of Claim 20, wherein the voltage supply is coupled between the first and second PFETs of the cross-coupled inverter.

22. (previously presented) The driver circuit of Claim 10, wherein the output buffers include one or more inverters.

23. (currently amended) A break-before-make predriver, comprising:

inverter means for receiving an input signal and inverting said input signal;

cross-coupled inverter means for providing a break-before-make delay, wherein the cross-coupled inverter means is configured to receive the output of the inverter means, and the cross-coupled inverter means is further configured to receive the input signal;

first and second output buffer means for receiving first and second outputs of the cross-coupled inverter means, for inverting the first output of the cross-coupled inverter means while leaving the second output of the cross-coupled inverter means uninverted so that the first output buffer means provides a break transition before the second output buffer means provides a make transition, and the second output buffer means provides a break transition before the first output buffer means provides a make transition; and

first and second tristate means for disabling output signals of the first and second predriver output nodes.

24. (canceled)

25. (previously presented) The predriver of Claim 23, further comprising:

voltage supply means for supplying a higher voltage at predriver output nodes than a voltage of the input signal.

26. (currently amended) In a circuit having an input inverter configured to receive an input signal, two cross-coupled inverters including a pair of NFETs and a pair of PFETs, and first and second output buffers, a sizing method for creating a break before make delay with substantially equal action on rising and falling edges, the method comprising:

sizing the NFETs and PFETs of the cross-coupled inverters such that the NFETs are larger than the PFETs of the cross-coupled inverters,

sizing the input inverter, the cross-coupled inverters and the first and second output buffers with respect to each other such that first and second delays between an input signal and predriver make signals on a rising and falling edge, respectively, are substantially equal;

sizing the input inverter, the cross-coupled inverters and the first and second output buffers with respect to each other such that an third and fourth delays between a break signal and make signal on a rising edge and falling edge, respectively, are substantially equal;

configuring the first and second output buffers such that the break signal on the rising edge occurs before the make signal on the rising edge, and the break signal on the falling edge occurs before the make signal on the falling edge; and

configuring the cross-coupled inverters to remove both the current source and the current sink from the load concurrently to allow tristate operation of the circuit.

27. (previously presented) The method as recited in Claim 26, further comprising:

sizing the input inverter, cross-coupled inverters and first and second output buffers according to specifications for driving a capacitive load.